AA6023A (V1.2)

- Feature

1. Single Game Size : C3: PRO : 128KB/256KB/512KB/1MB/2MB; PPU : 128KB/256K

   Low-K: PRO : 16KB/32KB; PPU : 8KB/16KB/32KB

2. Operation Voltage: 2.4V ~ 6.5V

3. CENB is chip enable, build-in pull-low resistor. If CENB="1" => POEB="1", IRQB="open", HV="open".

4. SELC3B = "0" (After Power On) => C3 mode; SELC3B = "1" => Low-K mode;

5. In Low-K mode, IRQB="1", HV="1".

6. K5K6 = NC -> REG6K(Compatible KP6022C) ; K5K6 = "1" -> REG5K

- Setting

1. REG$6000 / REG$5000 (x110-xxxx-xxxx-x000 / x101-xxxx-xxxx-x000) (WRITE ONLY, After POWER-ON, "0000-0000 - > D7--D0")

D7	D6	D5	D4	D3	D2	D1	D0
SELCA17	SELPA17	CA19B	CA18	`CA17	`PA19	`PA18	`PA17

* If SELCA17="0" => CA17=C3CA17; If SELCA17="1" => CA17=`CA17.

* If SELPA17="0" => PA17=C3PA17; If SELPA17="1" => PA17=`PA17.

2. REG$6001 / REG$5001 (x110-xxxx-xxxx-x001 / x101-xxxx-xxxx-x001) (WRITE, After POWER-ON, "0000-0000 - > D7--D0")

D7	D6	D5	D4	D3	D2	D1	D0
SELPA18	SELPA19*	SELPA20*	`PA20*	PX0*	PX1*	SELPA14	SC0

* If SELC3B="0" => PA13=C3PA13; If SELC3B="1" => PA13= A13.

* If SELC3B="0" => PA14=C3PA14; If SELC3B="1" & SELPA14="0" => PA14= `PA14; If SELC3B="1" & SELPA14="1" => PA14= A14.

* If SELPA18="0" => PA18=C3PA18; If SELPA18="1" => PA18=`PA18.

* If SELPA19="0" => PA19=`PA19; If SELPA19="1" => PA19= C3PA19.

* If SELPA20="0" => PA20=`PA20; If SELPA20="1" => PA20= C3PA20.

* PX0 & PX1 = OUTPUT to PX0 & PX1

3. REG$6002 / REG$6002 (x110-xxxx-xxxx-x010 / x101-xxxx-xxxx-x010) (WRITE ONLY, After POWER-ON, "0000-0000 - > D7--D0")

D7	D6	D5	D4	D3	D2	D1	D0
ODN	OD2	OD1	OD0	`CA16	`CA15	`CA14	`CA13

* If ODN="1" => LOCK OD0, OD1, OD2, until RESET or Power-Off.

* OD0 / OD1 / OD2 are enable signal of `CA14 / `CA15 / `CA16. Active Low.

4. REG$6003 / REG$5003 (x110-xxxx-xxxx-x011 / x101-xxxx-xxxx-x011) (WRITE ONLY, After POWER-ON, "0000-0000 - > D7--D0")

D7	D6	D5	D4	D3	D2	D1	D0
CEN	SEL23*	RAM256K*	SELC3B	`PA16	`PA15	`PA14	SC1

* If CEN="1" => LOCK REG$6000, REG$6001, REG$6003, REG$6004, REG$6005 until RESET or Power-Off.

* If SELC3B="0" => PA16/PA15=C3PA16/C3PA15; If SELC3B="1" => PA16/PA15=`PA16/`PA15.

* If SELC3B="0" => CA16/CA15/CA14/CA13=C3CA16/C3CA15/C3CA14/C3CA13; If SELC3B="1" => CA16/CA15/CA14/CA13=`CA16/`CA15/`CA14/`CA13.

* If SEL23*="0" => Compatible to KP6022C; If SEL23*="1" => C4 Decoder

* If RAM256K*="0" => Program SRAM:8KB; If RAM256K="1" => Program SRAM:12KB

5. REG$6004 / REG$5004 (x110-xxxx-xxxx-x100/ x101-xxxx-xxxx-x100) (WRITE ONLY, After POWER-ON, "0000-0000 - > D7--D0")

D7	D6	D5	D4	D3	D2	D1	D0
Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0

* Switch Addr. For GROMB & GRAMB

X1 = Q0 & (XVA11 xor Q1) ; X2 = XVA12 xor Q2 ; X3 = XVA13 xor Q3 ; X4 = XVA14 xor Q4

X5 = XVA15 xor Q5 ; X6 = XVA16 xor Q6 ; X7 = XVA17 xor Q7

Y1 = X1 + X2 + X3 + X4 + X5 + X6 + X7

GROMB = VCSB + Y1\ ; GRAMB = VCSB + Y1

6. REG$6005 / REG$5005 (x110-xxxx-xxxx-x101/ x101-xxxx-xxxx-x101) (WRITE , After POWER-ON, “0000-0000 - > D7--D0”)

D7	D6	D5	D4	D3	D2	D1	D0
--	--	--	K0	GSB	GSA	FSB	FSA

* FSB FSA Function

0 0 C3/C4 → FS0

0 1 IQ893L (GAL20L8 + Diode + Resistors) → FS1

1 0 IQ813L (TTL + Diode + Resistors) → FS2

* GSB GSA Function for GROM & GRAM

0 0 Use REG$x004 → GS0

0 1 Heavy Army** → GS1

Note: VA13 --> VA13B

1 0 2nd Time → GS2

If K0=”0”, PA18-OUT = PA18-IC ; PA19-OUT = PA19IC

K0=”1”, PA18-OUT = CA16 or A14 ; PA19-OUT = CA17 or A14

7. LOG813

A8	A6	A5	A4	A3	A2	A1	A0
XA19	XA18	XA17	XA16	XA15	S16K	SHV	SA14

SRAM at $6000.

LOG893

D7	D6	D5	D4	D3	D2	D1	D0
--	--	XA16	XA15	XVA16	XVA15	XVA14	XVA13

SRAM at $x11x-0xxx-xxxx-xxxx

For SHENHUO: IC:A0 = CPU:A8 ; IC:A1 = CPU:A11

For JINGKE: IC:A0 = CPU:A11 ; IC:A1 = CPU:A11

8. For dual menu: OA0, SL0, SC0, SC1

SC0	SC1	OA0
0	0	A0
0	1	1
1	0	SL0
1	1	SL0

9. Active LOG813 (Game: 8M-ROM + 7420 + 74273 + Resistor + Diode) :

a. Set FS2=1 => REG@6005=$02

b. Set REG@6002 = $80

c. Set REG@6003 = $80

d. 8M-ROM:A0-A14 to CPU:A0-A14

8M-ROM:A15-A19 to AA6023:PA15-PA19

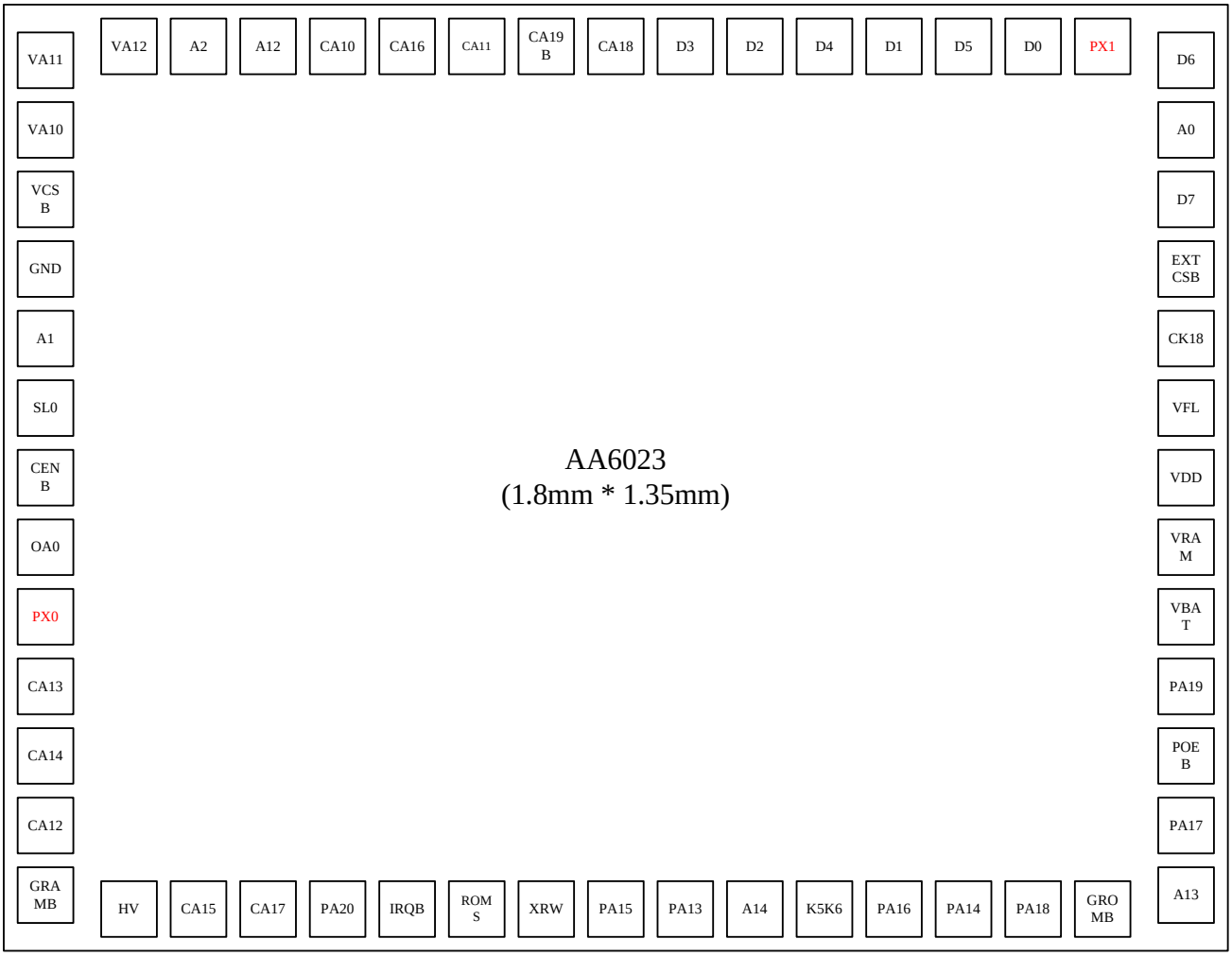
8M-ROM:OEB to GND ; 8M-ROM:CSB to AA6023 : POEB

PRO-SRAM:6264:WEB to CPU:R/W ; PRO-SRAM:6264:OEB to GND ; PRO-SRAM:6264 to AA6023:EXTCSB

PPU-SRAM-6264 to CPU

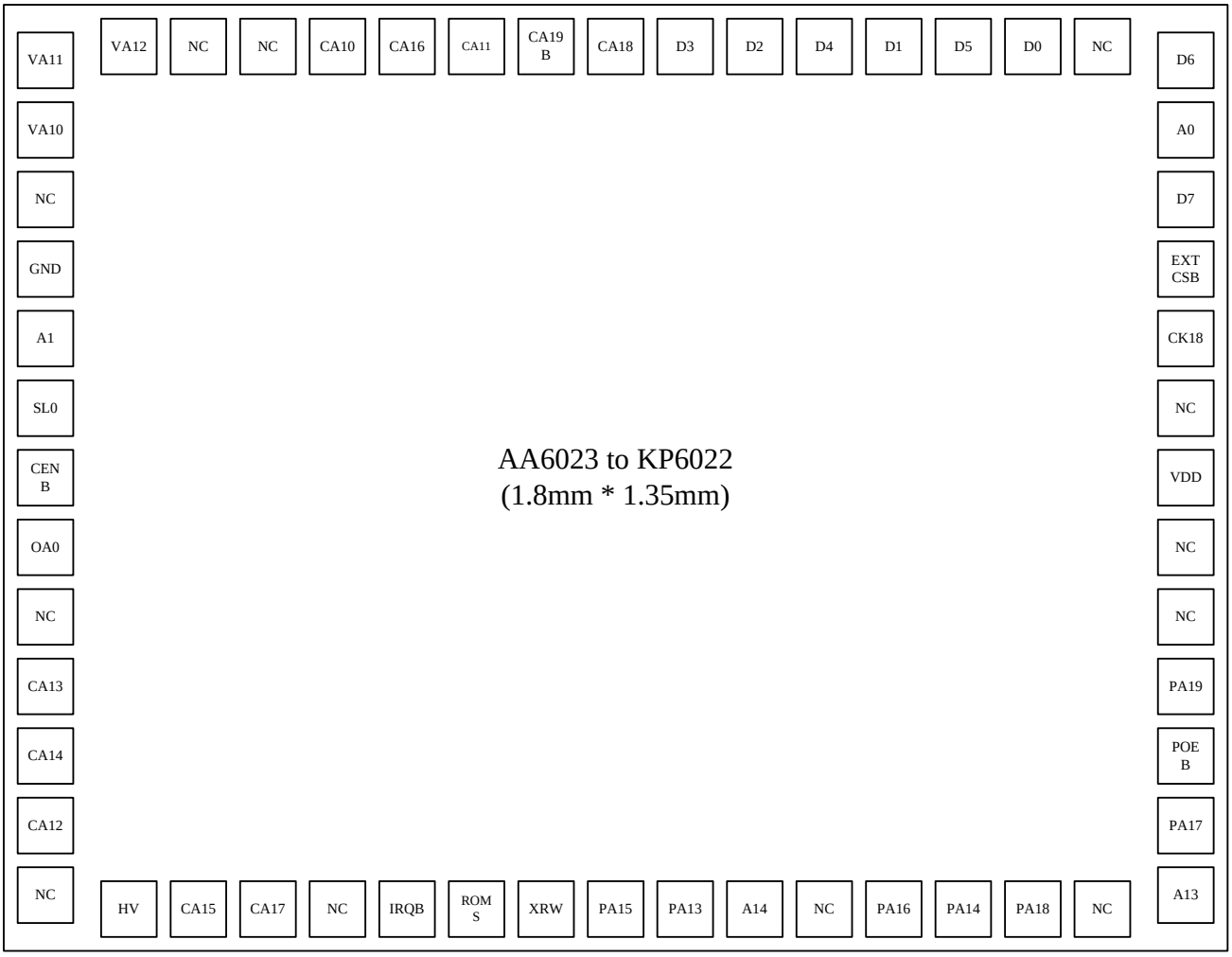
AA6023A BONDING PAD LOCATION

PIN	NAME	X	Y	PIN	NAME	X	Y	PIN	NAME	X	Y
1	VDD	786.55	0	21	A2	-552	562.5	41	ROMS	-184	-562.5
2	VFL	786.55	92	22	VA12	-644	562.5	42	XRW	-92	-562.5
3	CK18	786.55	184	23	VA11	-786.55	552	43	PA15	0	-562.5
4	EXTCSB	786.55	276	24	VA10	-786.55	460	44	PA13	92	-562.5
5	D7	786.55	368	25	VCSB	-786.55	368	45	A14	184	-562.5
6	A0	786.55	460	26	GND	-786.55	276	46	K5K6	276	-562.5
7	D6	786.55	552	27	A1	-786.55	184	47	PA16	368	-562.5
8	PX0	644	562.5	28	SL0	-786.55	92	48	PA14	460	-562.5
9	D0	552	562.5	29	CENB	-786.55	0	49	PA18	552	-562.5
10	D5	460	562.5	30	OA0	-786.55	-92	50	GROMB	644	-562.5
11	D1	368	562.5	31	PX1	-786.55	-184	51	A13	786.55	-552
12	D4	276	562.5	32	CA13	-786.55	-276	52	PA17	786.55	-460
13	D2	184	562.5	33	CA14	-786.55	-368	53	POEB	786.55	-368
14	D3	92	562.5	34	CA15	-786.55	-460	54	PA19	786.55	-276
15	CA18	0	562.5	35	GRAMB	-786.55	-552	55	VBAT	786.55	-184
16	CA19B	-92	562.5	36	HV	-644	-562.5	56	VRAM	786.55	-92
17	CA11	-184	562.5	37	CA15	-552	-562.5				
18	CA16	-276	562.5	38	CA17	-460	-562.5				
19	CA10	-368	562.5	39	PA20	-368	-562.5				
20	A12	-460	562.5	40	IRQB	-276	-562.5				



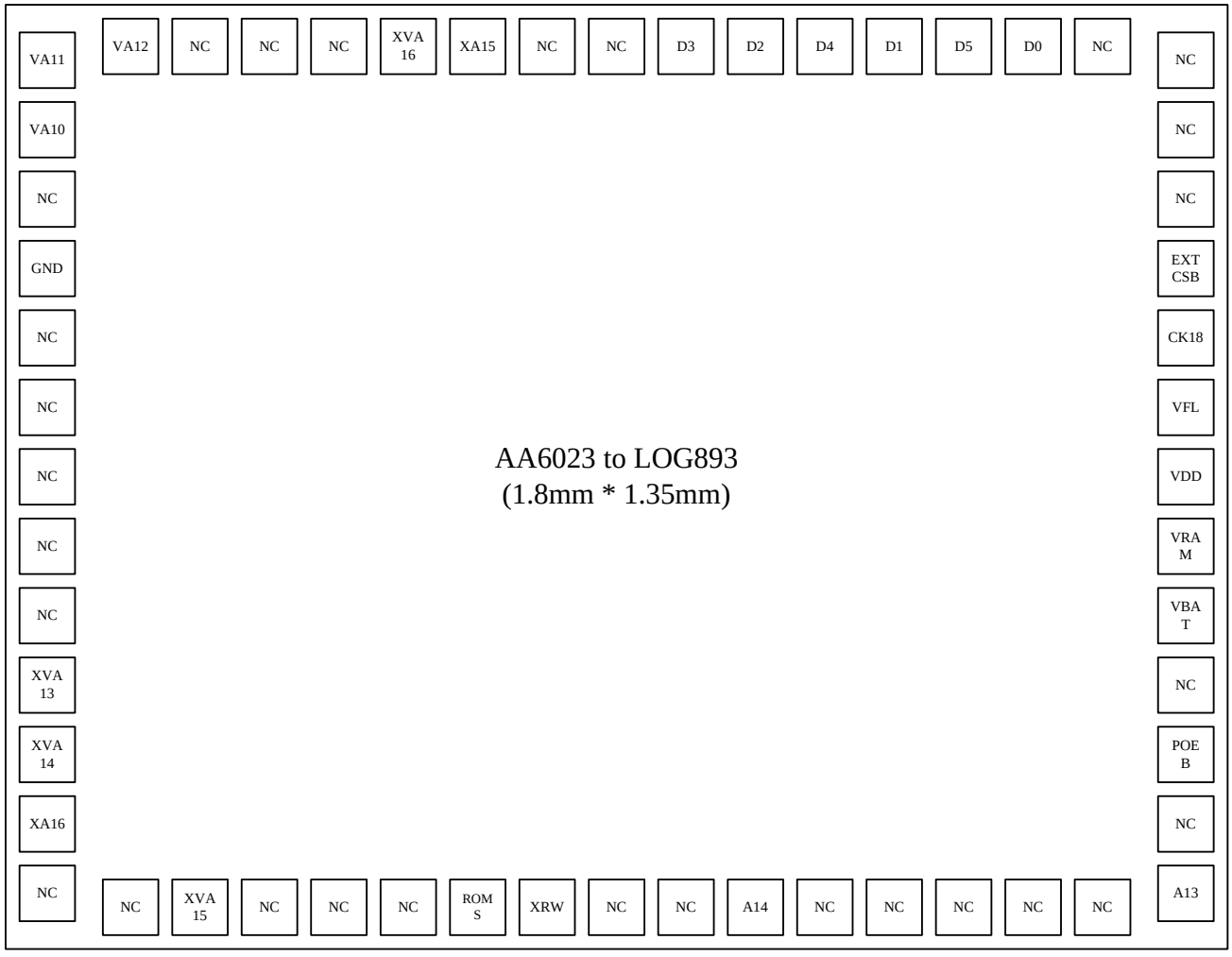
AA6023A for KP6022C BONDING PAD LOCATION

PIN	NAME	X	Y	PIN	NAME	X	Y	PIN	NAME	X	Y
1	VDD	786.55	0	21	A2	-552	562.5	41	ROMS	-184	-562.5
2	VFL	786.55	92	22	VA12	-644	562.5	42	XRW	-92	-562.5
3	CK18	786.55	184	23	VA11	-786.55	552	43	PA15	0	-562.5
4	EXTCSB	786.55	276	24	VA10	-786.55	460	44	PA13	92	-562.5
5	D7	786.55	368	25	VCSB	-786.55	368	45	A14	184	-562.5
6	A0	786.55	460	26	GND	-786.55	276	46	K5K6	276	-562.5
7	D6	786.55	552	27	A1	-786.55	184	47	PA16	368	-562.5
8	PX0	644	562.5	28	SL0	-786.55	92	48	PA14	460	-562.5
9	D0	552	562.5	29	CENB	-786.55	0	49	PA18	552	-562.5
10	D5	460	562.5	30	OA0	-786.55	-92	50	GROMB	644	-562.5
11	D1	368	562.5	31	PX1	-786.55	-184	51	A13	786.55	-552
12	D4	276	562.5	32	CA13	-786.55	-276	52	PA17	786.55	-460
13	D2	184	562.5	33	CA14	-786.55	-368	53	POEB	786.55	-368
14	D3	92	562.5	34	CA15	-786.55	-460	54	PA19	786.55	-276
15	CA18	0	562.5	35	GRAMB	-786.55	-552	55	VBAT	786.55	-184
16	CA19B	-92	562.5	36	HV	-644	-562.5	56	VRAM	786.55	-92
17	CA11	-184	562.5	37	CA15	-552	-562.5				
18	CA16	-276	562.5	38	CA17	-460	-562.5				
19	CA10	-368	562.5	39	PA20	-368	-562.5				
20	A12	-460	562.5	40	IRQB	-276	-562.5				



AA6023A—LOG893 BONDING PAD LOCATION

PIN	NAME	X	Y	PIN	NAME	X	Y	PIN	NAME	X	Y
1	VDD	786.55	0	21	A2	-552	562.5	41	ROMS	-184	-562.5
2	VFL	786.55	92	22	VA12	-644	562.5	42	XRW	-92	-562.5
3	CK18	786.55	184	23	VA11	-786.55	552	43	PA15	0	-562.5
4	EXTCSB	786.55	276	24	VA10	-786.55	460	44	PA13	92	-562.5
5	D7	786.55	368	25	VCSB	-786.55	368	45	A14	184	-562.5
6	A0	786.55	460	26	GND	-786.55	276	46	K5K6	276	-562.5
7	D6	786.55	552	27	A1	-786.55	184	47	PA16	368	-562.5
8	PX0	644	562.5	28	SL0	-786.55	92	48	PA14	460	-562.5
9	D0	552	562.5	29	CENB	-786.55	0	49	PA18	552	-562.5
10	D5	460	562.5	30	OA0	-786.55	-92	50	GROMB	644	-562.5
11	D1	368	562.5	31	PX1	-786.55	-184	51	A13	786.55	-552
12	D4	276	562.5	32	CA13	-786.55	-276	52	PA17	786.55	-460
13	D2	184	562.5	33	CA14	-786.55	-368	53	POEB	786.55	-368
14	D3	92	562.5	34	CA15	-786.55	-460	54	PA19	786.55	-276
15	CA18	0	562.5	35	GRAMB	-786.55	-552	55	VBAT	786.55	-184
16	CA19B	-92	562.5	36	HV	-644	-562.5	56	VRAM	786.55	-92
17	CA11	-184	562.5	37	CA15	-552	-562.5				
18	CA16	-276	562.5	38	CA17	-460	-562.5				
19	CA10	-368	562.5	39	PA20	-368	-562.5				
20	A12	-460	562.5	40	IRQB	-276	-562.5				



AA6023A to LOG813 BONDING PAD LOCATION

PIN	NAME	X	Y	PIN	NAME	X	Y	PIN	NAME	X	Y
1	VDD	786.55	0	21	A2	-552	562.5	41	ROMS	-184	-562.5
2	VFL	786.55	92	22	VA12	-644	562.5	42	XRW	-92	-562.5
3	CK18	786.55	184	23	VA11	-786.55	552	43	PA15	0	-562.5
4	EXTCSB	786.55	276	24	VA10	-786.55	460	44	PA13	92	-562.5
5	D7	786.55	368	25	VCSB	-786.55	368	45	A14	184	-562.5
6	A0	786.55	460	26	GND	-786.55	276	46	K5K6	276	-562.5
7	D6	786.55	552	27	A1	-786.55	184	47	PA16	368	-562.5
8	PX0	644	562.5	28	SL0	-786.55	92	48	PA14	460	-562.5
9	D0	552	562.5	29	CENB	-786.55	0	49	PA18	552	-562.5
10	D5	460	562.5	30	OA0	-786.55	-92	50	GROMB	644	-562.5
11	D1	368	562.5	31	PX1	-786.55	-184	51	A13	786.55	-552
12	D4	276	562.5	32	CA13	-786.55	-276	52	PA17	786.55	-460
13	D2	184	562.5	33	CA14	-786.55	-368	53	POEB	786.55	-368
14	D3	92	562.5	34	CA15	-786.55	-460	54	PA19	786.55	-276
15	CA18	0	562.5	35	GRAMB	-786.55	-552	55	VBAT	786.55	-184
16	CA19B	-92	562.5	36	HV	-644	-562.5	56	VRAM	786.55	-92
17	CA11	-184	562.5	37	CA15	-552	-562.5				
18	CA16	-276	562.5	38	CA17	-460	-562.5				
19	CA10	-368	562.5	39	PA20	-368	-562.5				
20	A12	-460	562.5	40	IRQB	-276	-562.5